## AMENDMENTS TO THE CLAIMS

Claim 1 (Previously Presented): In a processor having a plurality of kernel planes with a plurality of kernels for processing data in a communication device, at least one kernel of the plurality of kernels comprising:

an interface adapted to receive and transmit information from the at least one kernel;

a satellite kernel coupled to the interface, the satellite kernel performing a discrete class of operations within a communications application; and

a local controller coupled to the interface and the satellite kernel, and the local controller permitting the at least one kernel to operate autonomously with respect to the other of the plurality of kernels.

Claim 2 (Previously Presented): The processor recited in Claim 1 wherein the satellite kernel is configurable to perform a specific sub function within the class of sub functions.

Claim 3 (Previously Presented): The processor recited in Claim 1 wherein the satellite kernel is reconfigurable from a first sub function to perform a second sub function within the discrete class of operations.

Claim 4 (Previously Presented): The processor recited in Claim 1 wherein the satellite kernel is reconfigurable only within the class of operations.

Claim 5 (Previously Presented): The processor recited in Claim 1 wherein the satellite kernel includes a plurality of electronic devices for performing arithmetic, logic, and storage operations, the plurality of electronic devices coupled to each other and to the local controller in a fixed manner for implementing functions common to the class of operations, the plurality of electronic devices coupled to each other in a reconfigurable manner for implementing functions unique within the class of operations.

Claim 6 (Previously Presented): The processor recited in Claim 5 wherein the electronic devices are coupled to each other using a reconfigurable logic technique, a reconfigurable datapath technique, a reconfigurable dataflow technique, or a reconfigurable control technique for the discrete class of operations performed by the satellite kernel.

Claim 7 (Previously Presented): The processor recited in Claim 6 wherein the electronic devices are coupled to each other using a heterogeneous combination of the reconfigurable logic technique, the reconfigurable datapath technique, the reconfigurable dataflow technique, or the reconfigurable control technique.

Claim 8 (Previously Presented): The processor recited in Claim 4 wherein the reconfigurability of the at least one kernel is established on a temporal basis, a logical basis, or a functional basis.

Claim 9 (Previously Presented): The processor recited in Claim 8, wherein the class of operations is based upon a desired level of performance for the application.

Claim 10 (Previously Presented): The processor recited in Claim 1 wherein the discrete class of operations is an algorithm.

Claim 11 (Previously Presented): The processor recited in Claim 1, wherein the class of operations is limited to a class of mathematical field operations.

Claim 12 (Previously Presented): The processor recited in Claim 1, wherein the application within which the operations are used is a wireless communications application.

Claim 13 (Previously Presented): The processor recited in Claim 12, wherein the operations used in the wireless communications application include modem operations and codec operations.

Claim 14 (Currently Amended): The processor recited in Claim 1, wherein the local controller manages the satellite kernel autonomously from circuitry outside of the ~~computing element~~processor.

Claim 15 (Previously Presented): The processor recited in Claim 1 wherein the satellite kernel includes a computing element at a lower hierarchical level than the satellite kernel.

Claim 16 (Previously Presented): The processor recited in Claim 5 wherein the satellite kernel includes a plurality of selective interconnects coupling the plurality of electronic devices.

Claim 17 (Withdrawn): An electronic device having a discrete processor architecture, the communication device comprising:

a first computing element for performing a first discrete operation, or portion thereof, in an application;

a second computing element for performing a second discrete operation, or portion thereof, in the application; and

a reconfigurable interconnect coupled to the first computing element and the second computing element, wherein the first computing element, the second computing element, and the reconfigurable interconnect are operable to perform a class of functions within an application.

Claim 18 (Withdrawn): The electronic device recited in Claim 17, wherein the first computing element and the second computing element are heterogeneous with respect to each other in terms of programming granularity.

Claim 19 (Withdrawn): The electronic device recited in Claim 17 wherein the first computing element and the second computing element are heterogeneous in terms of levels of millions of operations (MOPs) capacity.

Claim 20 (Withdrawn): The electronic device recited in Claim 17 further comprising a scheduler state machine coupled to the first computing element and to the second configurable element, the scheduler state machine sequencing the first discrete operation of the first computing element and the second discrete operation of the second computing element in parallel or in series to implement the function.

Claim 21 (Withdrawn): The electronic device recited in Claim 17 wherein the reconfigurable interconnect has an uncommitted architecture.

Claim 22 (Withdrawn): The electronic device recited in Claim 17 wherein the reconfigurable interconnect has a restricted amount of interconnections between the first computing element and the second computing element, the restricted amount of interconnections proportional to a variation within the class of functions in the application.

Claim 23 (Withdrawn): The electronic device recited in Claim 17 wherein the reconfigurable interconnect couples a quantity of input/output lines from the first computing element with a quantity of input/output lines from the second computing element in a manner that is defined by a rule set, the rule set representing a communication processing function.

Claim 24 (Withdrawn): The electronic device recited in Claim 17 wherein the reconfigurable interconnect is a programmable bus channel.

Claim 25 (Withdrawn): The electronic device recited in Claim 17 wherein the reconfigurable interconnect has a reconfigurable logic configuration.

Claim 26 (Withdrawn): The electronic device recited in Claim 17 wherein the reconfigurable interconnect is reconfigurable on a temporal basis, a logical basis, or a functional basis.

Claim 27 (Withdrawn): The electronic device recited in Claim 26 wherein the reconfigurable interconnect has a plurality of configurations that couple the first computing element and the second computing element, the plurality of configurations of the reconfigurable interconnect varying in time.

Claim 28 (Withdrawn): The electronic device recited in Claim 17 wherein the first computing element and the second computing element can operate in a plurality of modes.

Claim 29 (Withdrawn): The electronic device recited in Claim 17 wherein the class of functions is for a modem function in a wireless communication application.

Claim 30 (Withdrawn): The electronic device recited in Claim 17 wherein the class of functions is for a codec function in a wireless communication application.

Claim 31 (Withdrawn): The electronic device recited in Claim 18 wherein the first computing element, the second computing element, and the reconfigurable interconnect are configurable to perform a specific function defined within the class of functions of the application.

Claim 32 (Withdrawn): The electronic device recited in Claim 17 further comprising a plurality of computing elements, wherein each of the plurality of elements have at least one line selectively coupled to the reconfigurable interconnect.

Claim 33 (Withdrawn): The electronic device recited in Claim 31, wherein the class of functions is based upon a level of performance for the application.

Claim 34 (Withdrawn): The electronic device recited in Claim 33, wherein the level of performance is a symbol-based level of performance.

Claim 35 (Withdrawn): The electronic device recited in Claim 33, wherein the level of performance is based on millions of operations per second (MOPS).

Claim 36 (Withdrawn): The electronic device recited in Claim 33, wherein the level of performance is based on a type of mathematics for the application.

Claim 37 (Withdrawn): An electronic spread spectrum communication device for processing data, the electronic spread spectrum communication device comprising:

a channel card having a plurality of autonomous computing elements coupled to each other via a configurable interconnect;

a processor coupled to the channel card, the processor operable to convey instructions and data to the channel card; and

a computer readable memory unit coupled to the processor and to the channel card, the computer readable memory unit operable to store reconfiguration data.

Claim 38 (Withdrawn): The electronic spread spectrum communication device recited in Claim 37 wherein the channel card performs a modem function.

Claim 39 (Withdrawn): The electronic spread spectrum communication device recited in Claim 37 wherein the channel card performs a codec function.

Claim 40 (Withdrawn): The electronic spread spectrum communication device recited in Claim 37 wherein the channel card is reconfigurable to perform functions for any one of a plurality of communication protocols.

Claim 41 (Withdrawn): The electronic spread spectrum communication device recited in Claim 37 wherein each of the autonomous computing elements is operable only within a class of communication functions for which they were designed.

Claim 42 (Withdrawn): The electronic spread spectrum communication device recited in Claim 37 further comprising an additional channel card having multiple levels of programming granularity, the additional channel card operable to perform a modem function.

Claim 43 (Withdrawn): The electronic spread spectrum communication device recited in Claim 37 further comprising a channel card controller, the controller card operable to enable configuration of portions of the channel card.

Claim 44 (Withdrawn): The electronic spread spectrum communication device recited in Claim 37 further comprising an antenna interface, the antenna interface operable to provide a signal from each of a plurality of antennas to the channel card.

Claim 45 (Withdrawn): The electronic spread spectrum communication device recited in Claim 37 further comprising a digital signal processor (DSP) coupled to the channel card.

Claim 46 (Withdrawn): The electronic spread spectrum communication device recited in Claim 37 further comprising a programmable digital signal processor (DSP).

Claim 47 (Withdrawn): The electronic spread spectrum communication device recited in Claim 37 wherein the electronic spread spectrum communication device is a base transceiver station.

Claim 48 (Withdrawn): The electronic spread spectrum communication device recited in Claim 37 wherein the electronic spread spectrum communication device is a cellular handset.

Claim 49 (Withdrawn): The electronic spread spectrum communication device recited in Claim 37 wherein the electronic spread spectrum communication device is a cellular system test platform.

Claim 50 (Withdrawn): The electronic spread spectrum communication device recited in Claim 37 further comprising a base transceiver station cell controller.

Claim 51 (Previously Presented): A computer readable medium containing therein computer readable codes that enable an electronic device to access at least one kernel architecture of a plurality of kernel architectures in one of a plurality of kernel plane architectures, the method comprising:

reading an interface architecture, the interface architecture adapted to receive and transmit information from the at least one kernel architecture;

reading a satellite kernel architecture, the satellite kernel architecture coupled to the interface architecture, the satellite kernel architecture performing a discrete class of operations within a communications application; and

reading a local controller architecture, the local controller architecture being coupled to the interface architecture and the satellite kernel architecture and permitting the at least one kernel architecture to operate autonomously with respect to other of the plurality of kernel architectures.

Claim 52 (Previously Presented): The computer readable medium recited in Claim 51 wherein the satellite kernel architecture is configurable to perform a specific sub function within the class of sub functions.

Claim 53 (Previously Presented): The computer readable medium recited in Claim 51 wherein the satellite kernel architecture is reconfigurable from a first sub function to perform a second sub function within the discrete class of operations.

Claim 54 (Previously Presented): The computer readable medium recited in Claim 51 wherein the satellite kernel architecture is reconfigurable only within the class of operations.

Claim 55 (Previously Presented): The computer readable medium recited in Claim 51 wherein the satellite kernel architecture includes a plurality of electronic devices for performing arithmetic, logic, and storage operations, the plurality of electronic devices coupled to each other and to the local controller architecture in a fixed manner for implementing functions common to the class of

operations, the plurality of electronic devices coupled to each other in a reconfigurable manner for implementing functions unique within the class of operations.

Claim 56 (Original): The computer readable medium recited in Claim 55 wherein the electronic devices are coupled to each other using a reconfigurable logic technique, a reconfigurable datapath technique, a reconfigurable dataflow technique, or a reconfigurable control technique for the discrete class of operations performed by the satellite kernel.

Claim 57 (Original): The computer readable medium recited in Claim 56 wherein the electronic devices are coupled to each other using a heterogeneous combination of the reconfigurable logic technique, the reconfigurable datapath technique, the reconfigurable dataflow technique, or the reconfigurable control technique.

Claim 58 (Previously Presented): The computer readable medium recited in Claim 54 wherein the reconfigurability of the at least one kernel architecture is established on a temporal basis, a logical basis, or a functional basis.

Claim 59 (Original): The computer readable medium recited in Claim 51 wherein the class of operations is based upon a desired level of performance for the application.

Claim 60 (Previously Presented): The computer readable medium recited in Claim 51 wherein the discrete class of operations is an algorithm.

Claim 61 (Original): The computer readable medium recited in Claim 51 wherein the class of operations is limited to a class of mathematical field operations.

Claim 62 (Original): The computer readable medium recited in Claim 51, wherein the application within which the operations are used is a wireless communications application.

Claim 63 (Original): The computer readable medium recited in Claim 62, wherein the operations used in the wireless communications application include modem operations and codec operations.

Claim 64 (Currently Amended): The computer readable medium recited in Claim 51, wherein the local controller architecture manages the ~~satallite~~ satellite kernel architecture autonomously from circuitry outside of the ~~computing element architecture~~electronic device.

Claim 65 (Previously Presented): The computer readable medium recited in Claim 51 wherein the satellite kernel architecture includes a computing element architecture at a lower hierarchical level than the satellite kernel architecture.

Claim 66 (Currently Amended): The ~~computing element~~computer readable medium recited in Claim 55 wherein the satellite kernel architecture includes a plurality of selective interconnects coupling the plurality of electronic devices.

Claim 67 (Withdrawn): A computer readable medium containing therein computer readable codes that enable an electronic device to access an electronic circuit architecture, the method comprising:

reading a first computing element architecture, the first computing element architecture for performing a first discrete operation, or portion thereof, in an application;

reading a second computing element architecture for performing a second discrete operation, or portion thereof, in the application; and

reading a reconfigurable interconnect coupled to the first computing element and the second computing element, wherein the first computing element, the second computing element, and the reconfigurable interconnect are operable to perform a class of functions within an application.

Claim 68 (Withdrawn): The computer readable medium recited in Claim 67, wherein the first computing element and the second computing element are heterogeneous with respect to each other in terms of programming granularity.

Claim 69 (Withdrawn): The computer readable medium recited in Claim 67 wherein the first computing element and the second computing element are heterogeneous in terms of levels of millions of operations (MOPs) capacity.

Claim 70 (Withdrawn): The computer readable medium recited in Claim 67 wherein the hardware kernel architecture further comprises:

a scheduler state machine coupled to the first computing element and to the second configurable element, the scheduler state machine sequencing the first discrete operation of the first computing element and the second discrete operation of the second computing element in parallel or in series to implement the function.

Claim 71 (Withdrawn): The computer readable medium recited in Claim 67 wherein the reconfigurable interconnect has an uncommitted architecture.

Claim 72 (Withdrawn): The computer readable medium recited in Claim 67 wherein the reconfigurable interconnect has a restricted amount of interconnections between the first computing element and the second computing element, the restricted amount of interconnections proportional to a variation within the class of functions in the application.

Claim 73 (Withdrawn): The computer readable medium recited in Claim 67 wherein the reconfigurable interconnect couples a quantity of input/output lines from the first computing element with a quantity of input/output lines from the second computing element in a manner that is defined by a rule set, the rule set representing a communication processing function.

Claim 74 (Withdrawn): The computer readable medium recited in Claim 67 wherein the reconfigurable interconnect is a programmable bus channel.

Claim 75 (Withdrawn): The computer readable medium recited in Claim 67 wherein the reconfigurable interconnect has a reconfigurable logic configuration.

Claim 76 (Withdrawn): The computer readable medium recited in Claim 67 wherein the reconfigurable interconnect is reconfigurable on a temporal basis, a logical basis, or a functional basis.

Claim 77 (Withdrawn): The electronic device recited in Claim 67 wherein the class of functions is for a modem function in a wireless communication application.

Claim 78 (Withdrawn): The electronic device recited in Claim 68 wherein the class of functions is for a codec function in a wireless communication application.

Claim 79 (Withdrawn): The electronic device recited in Claim 69 wherein the first computing element, the second computing element, and the reconfigurable interconnect are configurable to perform a specific function defined within the class of functions of the application.

Claim 80 (Withdrawn): The electronic device recited in Claim 70 further comprising a plurality of computing elements, wherein each of the plurality of elements have at least one line selectively coupled to the reconfigurable interconnect.

Claim 81 (Withdrawn): The electronic device recited in Claim 79, wherein the class of functions is based upon a level of performance for the application.

Claim 82 (Withdrawn): The electronic device recited in Claim 81, wherein the level of performance is a symbol-based level of performance.

Claim 83 (Withdrawn): The electronic device recited in Claim 81, wherein the level of performance is based on millions of operations per second (MOPS).

Claim 84 (Withdrawn): The electronic device recited in Claim 81, wherein the level of performance is based on a type of mathematics for the application.

Claim 85 (Withdrawn): A method of implementing a design configuration on a configurable electronic device having a plurality of function-specific computing elements, the method comprising the steps of:

a) receiving the design configuration at the configurable electronic device;

b) determining a radio configuration desired for a channel element to be processed on the configurable electronic device; and

c) loading the design configuration software into control registers for the configurable electronic device.

Claim 86 (Withdrawn): The method recited in Claim 85 further comprising the step of:

d) loading an OSI software stack in the controller for the configurable electronic device.

Claim 87 (Withdrawn): The method recited in Claim 86 further comprising the step of:

d) interfacing the OSI software stack with an application programming software interface (API) to enhance signal processing of reconfigurable electronic device.

Claim 88 (Withdrawn): The method recited in Claim 86 further comprising the step of:

d) loading a specific configuration for each channel element into a digital signal processing (DSP).

Claim 89 (Withdrawn): The method recited in Claim 85 wherein steps a) through c) are accomplished dynamically on the configurable electronic device.

Claim 90 (Withdrawn): The method recited in Claim 85 wherein steps a) through c) are accomplished in parallel for time-sharing components of the configurable electronic device.

Claim 91 (Withdrawn): A method of operating a configurable electronic device with function-specific computing elements to communicate with another electronic device, the method comprising the steps of:

a) receiving a signal at the configurable electronic device;

b) assigning a data pump path for the signal in a configurable modem portion of the configurable electronic device;

c) receiving design configuration information for the configurable modem platform that is applicable communication protocol for the signal; and

d) performing digital signal processing of the data portion of the signal, using the reconfigurable modem platform, wherein the reconfigurable modem platform having a heterogeneous structure.

Claim 92 (Withdrawn): The method recited in Claim 91 further comprising the step of:

e) disassembling the signal into a data portion and a control portion using an interface section.

Claim 93 (Withdrawn): The method recited in Claim 91 further comprising the step of.

e) synchronizing the reconfigurable modem device with over the air timing.

Claim 94 (Withdrawn): The method recited in Claim 91 further comprising the following steps:

e) demuxing the signal processed by the reconfigurable modem platform; and

f) transmitting the signal from the modem platform for subsequent processing.

Claim 95 (Withdrawn): The method recited in Claim 91 further comprising the following steps of:

e) combining the signals to create composite signals on a per-sector and per-carrier basis using an interface section; and

f) formatting the composite signal using the interface section.

Claim 96 (Withdrawn): The method recited in Claim 91 wherein the digital signal processing in step d) includes performing codec functions using a reconfigurable codec chip having a heterogeneous structure.

Claim 97 (Withdrawn): The method recited in Claim 91 wherein the digital signal processing in step d) includes performing modem function using a reconfigurable modem chip having a heterogeneous structure.

Claim 98 (Withdrawn): The method recited in Claim 91 further comprising the steps of.

e) assembling payload data with control information; and

f) transmitting the payload data and control information to a mobile telephone switching office (MTSO).